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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/816,450	CHUN ET AL.	
	Examiner	Art Unit	
	BENJAMIN P. GEIB	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-11 and 17-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-11 and 17-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4, 7-11, 17-20, 22-27, 29, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alsolaim et al., "Architecture and Application of a Dynamically Reconfigurable Hardware Array for Future Mobile Communication Systems", (Hereinafter Alsolaim) in view of Henry, U.S. Patent No. 4,791,603.

3. Referring to claim 1, Alsolaim has taught an apparatus, comprising:

a memory unit *[dual port RAMs; Fig. 3]* to store input data for a plurality of functions *[last paragraph of section 3.1 on page 209]*, wherein each function comprises computationally intensive a communications signal processing task *[section 3.1, 1st paragraph]*;

a control unit *[RPU-controller; Fig. 3]* having a control unit state machine module to control execution of said plurality of functions *[1st full paragraph on page 209 and 2nd paragraph of left column on page 210]*, said control unit to select a function to execute using a function identifier *[Since the RPU-controller guides all operations, it inherently must select a function (i.e. operation) using a function identifier]*;

a configuration memory *[Alsolaim; Configuration Memory Unit (CMU)]* to store configuration parameters for said control unit, said configuration parameters including table content data *[Alsolaim; 1st full paragraph, left column, on page 208]*; and

a plurality of execution units *[RAP units; Figs. 3 & 4]* operatively responsive to said control unit, said execution units to receive input data from said memory unit, and use said input data to execute a function corresponding to said function identifier *[section 3.2]*.

Alsolaim has not explicitly taught that the control unit having a control unit state machine module is configured with a fuse map and that the configuration memory stores the fuse map.

Henry has taught configuring logic (i.e. a state machine module) using a fuse map *[Henry; column 2, lines 14-31; column 3, lines 44-66]*.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Alsolaim so that the control unit state machine module is configured using a fuse map. Because the control unit state machine is configured using the configuration parameters included in the configuration memory and, in the modified system, the fuse map is one of the configuration parameter, it would have been obvious to store the fuse map in the configuration memory.

The motivation for doing so would have been that the hardware is made more versatile *[Henry; column 2, lines 32-43]*.

4. Referring to claim 2, Alsolaim and Henry have taught the apparatus of claim 1, wherein said execution units comprise a logic unit to perform scalar arithmetic operations, and at least one data path execution unit to perform arithmetic operations *[Alsolaim; section 3.2]*.

5. Referring to claim 4, Alsolaim and Henry have taught the apparatus of claim 1, wherein said control unit comprises: said control unit state machine module to be configured in accordance with said fuse map, said control unit state machine to output an operation number address; and a control unit lookup table to be configured with said table content data, said control unit lookup table to convert said operation number address to a reconfigurator vector, said reconfigurator vector to control execution of said function by said execution units *[section 3.1]*.

6. Referring to claim 7, Alsolaim and Henry have taught the apparatus of claim 1, further comprising a data selector to read said input data from said memory unit, and distribute said input data to said execution units *[data router; Fig. 3]*.

7. Referring to claim 8, Alsolaim and Henry have taught the apparatus of claim 1, further comprising a register file module to store previously read input data during function execution when multiple read cycles are needed to provide data for said function *[dual port RAMs; Fig. 3; last paragraph of section 3.1 on page 209]*.

8. Referring to claim 9, Alsolaim and Henry have taught the apparatus of claim 1, further comprising a data packer to receive processed input data from said execution units, and to send said processed input data to an output buffer *[1st full paragraph on page 211]*.

9. Referring to claim 10, Alsolaim and Henry have taught the apparatus of claim 1, further comprising a data router adapter to communicate packets with said routing elements, said data router adapter to distribute data from received packets to said configuration memory or said memory unit, and transmit packets of processed data from said execution units stored in an output buffer *[1st full paragraph on page 211]*.

10. Referring to claim 11, Alsolaim and Henry have taught the apparatus of claim 2, wherein said logic unit comprises a data address generator to control writing said input data to said memory unit, and reading said input data from said memory unit *[section 3.2]*.

11. Referring to claims 17 and 24, taking claim 24 as exemplary, Alsolaim has taught an article comprising:

a storage medium; said storage medium including stored instructions that, when executed by a processor, result in receiving configuration parameters for a control unit, said configuration parameters including table content data *[1st full paragraph, left column, on page 208]*, configuring said control unit having a control unit state machine module *[RPU-controller; Fig. 3]* using said configuration parameters, receiving input data for a plurality of functions, wherein each function comprises a computationally intensive communications signal processing task *[section 3.1, 1st paragraph]*; controlling execution of said plurality of functions using control signals, and executing said plurality of functions by a plurality of execution units using said input data in accordance with said control signals *[1st full paragraph on page 209 and 2nd paragraph of left column on page 210]*.

Alsolaim has not explicitly taught that the configuration information includes a fuse map and that the configuration memory stores the fuse map.

Henry has taught configuring logic (i.e. a state machine module) using a fuse map *[Henry; column 2, lines 14-31; column 3, lines 44-66]*.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to modify Alsolaim so that the configuration information includes a fuse map. Because the control unit state machine is configured using the configuration parameters included in the configuration memory and, in the modified system, the fuse map is one of the configuration parameter, it would have been obvious to store the fuse map in the configuration memory.

The motivation for doing so would have been that the hardware is made more versatile *[Henry; column 2, lines 32-43]*.

12. Referring to claims 18 and 25, taking claim 25 as exemplary, Alsolaim and Henry have taught the article of claim 24, wherein the stored instructions, when executed by a processor, further result in said plurality of functions being executed during different time periods *[section 3.2]*.

13. Referring to claims 19 and 26, taking claim 26 as exemplary, Alsolaim and Henry have taught the article of claim 24, wherein the stored instructions when executed by a processor, further result in said configuring by configuring said control unit state machine module using said fuse map, and configuring a control unit lookup table using said table content data *[1st full paragraph on page 208]*.

14. Referring to claims 20 and 27, taking claim 27 as exemplary, Alsolaim and Henry have taught the article of claim 24, wherein the stored instructions when executed by a processor, further result in said controlling by reading a function identifier from a function list, generating a reconfigurator vector using said function identifier, sending a data select signal to a data selector to read input data from an input buffer in accordance with said reconfigurator vector, and sending function control signals to said execution units to process said input data in accordance with said reconfigurator vector *[section 3.1]*.

15. Referring to claims 22 and 29, taking claim 29 as exemplary, Alsolaim and Henry have taught the article of claim 24, wherein the stored instructions, when executed by a processor, further result in said executing by receiving said input data at said execution units, receiving function control signals from said control unit, and processing said received input data in accordance with said function control signals *[section 3.2]*.

16. Referring to claims 23 and 30, taking claim 30 as exemplary, Alsolaim and Henry have taught the article of claim 24, wherein the stored instructions, when executed by a processor, further result in said

receiving by receiving a function identifier and an input identifier for each function, creating an input buffer corresponding to each input identifier, and writing input data for each function in said corresponding input buffer *[section 3.2]*.

17. Claims 5, 6, 21, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Alsolaim in view of Henry, and further in view of Fette et al., U.S. Patent No. 4,862,407 (Hereinafter Fette).

18. Referring to claim 5, Alsolaim and Henry have taught the apparatus of claim 4.

Alsolaim and Henry have not explicitly taught wherein said control unit further comprises: an inner loop counter to count a number of repetitions of instructions in an inner loop, said inner loop counter to output an inner terminal count signal; an outer loop counter to count a number of repetitions of instructions in an outer loop, said outer loop counter to output an outer terminal count signal; and a register file module to store a state for one function while another function is being executed by said execution units.

Fette has taught a control unit comprising: an inner loop counter to count a number of repetitions of instructions in an inner loop, said inner loop counter to output an inner terminal count signal *[Fette; column 7, lines 31-38]*; an outer loop counter to count a number of repetitions of instructions in an outer loop, said outer loop counter to output an outer terminal count signal *[Fette; column 7, lines 31-38]*; and a register file module to store a state for one function while another function is being executed by said execution units *[Fette; function register (component 80); column 8, lines 8-13]*.

At the time the invention was made it would have been obvious to one of ordinary skill in the art to modify Alsolaim and Henry so that the control unit further comprises: an inner loop counter to count a number of repetitions of instructions in an inner loop, said inner loop counter to output an inner terminal count signal; an outer loop counter to count a number of repetitions of instructions in an outer loop, said outer loop counter to output an outer terminal count signal; and a register file module to store a state for one function while another function is being executed by said execution units as taught by Fette.

The motivation for doing so would have been to assist in the execution in the execution of loops *[Fette; column 7, lines 31-38]*.

19. Referring to claim 6, Alsolaim and Henry have taught the apparatus of claim 5.

Alsolaim and Henry have not explicitly taught wherein said control unit state machine module receives as inputs said inner terminal count signal, said outer terminal count signal, said function identifier, a current state index value, and status register values from said execution units, and uses said inputs to generate said operation number address.

Fette has taught a control unit that receives as inputs said inner terminal count signal, said outer terminal count signal, said function identifier, a current state index value, and status register values from said execution units, and uses said inputs to generate said operation number address *[Fette; column 8, lines 8-29]*.

At the time the invention was made it would have been obvious to one of ordinary skill in the art to modify Alsolaim and Henry so that the control unit state machine module receives as inputs said inner terminal count signal, said outer terminal count signal, said function identifier, a current state index value, and status register values from said execution units, and uses said inputs to generate said operation number address as taught by Fette.

The motivation for doing so would have been to assist in the execution in the execution of loops *[Fette; column 7, lines 31-38]*.

20. Referring to claims 21 and 28, taking claim 28 as exemplary, Alsolaim and Henry have taught the article of claim 27.

Alsolaim and Henry have not explicitly taught wherein the stored instructions, when executed by a processor, further result in said generating by receiving as inputs an inner terminal count signal, an outer terminal count signal, said function identifier, a current state index value, and status register values from said execution units, at said control unit state machine, generating an operation number address using said inputs, converting said operation number address to a reconfigurator vector, said reconfigurator vector to control execution of said function by said execution units.

Fette has taught stored instructions, when executed by a processor, further result in said generating by receiving as inputs an inner terminal count signal, an outer terminal count signal, said function identifier, a current state index value, and status register values from said execution units, at said control unit state machine, generating an operation number address using said inputs, converting said operation number address to a reconfigurator vector, said reconfigurator vector to control execution of said function by said execution units *[Fette; column 7, lines 31-38]*.

At the time the invention was made it would have been obvious to one of ordinary skill in the art to modify Alsolaim and Henry so that the stored instructions, when executed by a processor, further result in said generating by receiving as inputs an inner terminal count signal, an outer terminal count signal, said function identifier, a current state index value, and status register values from said execution units, at said control unit state machine, generating an operation number address using said inputs, converting said operation number address to a reconfigurator vector, said reconfigurator vector to control execution of said function by said execution units as taught by Fette.

The motivation for doing so would have been to assist in the execution in the execution of loops *[Fette; column 7, lines 31-38]*.

Response to Arguments

21. Applicant's arguments filed 11/28/2009 have been fully considered but they are not persuasive.

22. Applicant argues the novelty/rejection of the claims, in substance, that: "Alsolaim fails to disclose, teach, or suggest at least wherein each function comprises a computationally intensive communications signal processing task." See page 9 of remarks. Applicant asserts that Alsolaim "merely teaches a simple operation such as addition or subtraction." See page 9 or remarks. The Examiner disagrees with this assertion and notes that the Applicant appears to be reading the phrase "computationally intensive communications signal processing task" too narrowly. The Applicant has not defined "computationally intensive" such that a particular level of computation is required and, therefore, the phrase entitled to its broadest reasonable interpretation. As understood by one of ordinary skill in the art, operations such as

addition and subtraction are computationally intensive in that relative to operations like AND and OR they involve many more logical computations. Furthermore, in addition to performing addition and subtraction, Alsolaim has taught performing even more computationally intensive functions or operations, such as multiplication, division, and multiply-and-accumulate (MAC). See Alsolaim; Table 1 on page 209. Therefore, Alsolaim has taught "wherein each function comprises a computationally intensive communications signal processing task."

Conclusion

23. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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